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SiSoft™ Announces Support for Design of Experiments (DoE) Flows with Interface to JMP®

Support for Design of Experiments Flow Accelerates Design Processes by Allowing Designers to Explore Extremely Large Design Spaces Quickly and Efficiently

Santa Clara, CA – January 28, 2013 - Signal Integrity Software, Inc. (SiSoft™) today announced that it has developed an interface to SAS' JMP® statistical discovery software that for the first time lets high-speed system designers characterize extremely large design spaces to make informed engineering decisions.

The use of statistical discovery techniques for high-speed signal integrity analysis solves two critical problems with traditional design flows:

- Cascaded min/max (guardband) analysis is overly conservative, predicting negative design margins even when their probability of occurrence is extremely low. These techniques can predict a design will fail even when the real-world success rate exceeds 99.99%.
- Design spaces expand exponentially as the number of parameters to be studied are increased. For a design with 10 variable parameters, each having 5 possible values, over 9.7 *million* simulations are required to explore the design space with conventional methods. Statistical discovery methods can provide comparable results even with as few as 2,000 simulations.

SiSoft's integrated flow for design of experiments (DoE) consists of 4 separate design and analysis steps:

1. The design creates a schematic topology of the circuit to be studied and identifies key design parameters as variables, which are automatically exported to JMP.
2. JMP is used to identify the design space to be explored, automatically reducing the number of simulations required by a factor of 100 to 5,000.
3. The simulation experiments are automatically run by [Quantum Channel Designer®](#) (QCD), SiSoft's Multi-Gigabit serial link analysis software or [Quantum-SI™](#) (QSI), SiSoft's automated DDR2/3/4 signal integrity and timing analysis software.
4. Simulation results are automatically loaded back into JMP software's statistical model, which can then be used to predict behavior under millions of different combinations of conditions, developing a comprehensive view of how the design will behave under real-world conditions.

SiSoft collaborated with software developers from JMP to design the integrated DoE flow, which will be used to explore extremely large design spaces associated with DDR4 and Multi-gigabit serial link designs. Until now, users have created their own in-house flows that are

hard to scale across companies. By enabling a statistical discovery flow for signal integrity applications, SiSoft is making these techniques available to the mainstream signal integrity market.

“The Design of Experiments flow is equally applicable for both serial and parallel design applications,” noted Barry Katz, SiSoft’s President and CTO. “Serial link designs have many different design parameters, necessitating this type of approach. With DDR4, conventional cascaded analysis techniques uniformly yield negative design margins that are needlessly pessimistic, with statistical discovery being the only way to reasonably predict the distribution of real-world design behavior. In each case, the many simulations still required are an ideal match for SiSoft’s simulation farm acceleration, which leverages the power of multiple simulation cores to reduce simulation run times.”

The Design of Experiments simulation flow is being demonstrated on the show floor this week at DesignCon and will be available with SiSoft’s upcoming 2013.03 software release.

About SiSoft™

SiSoft collaborates with customers and their suppliers to develop innovative solutions to the world’s toughest high-speed design problems. SiSoft accelerates design cycles through a combination of award-winning EDA simulation software, methodology training and consulting services. Quantum Channel Designer (QCD) is the Industry’s Premier Channel Simulator for the design and analysis of Multi-Gigabit serial links and a DesignVision Award Winner. Quantum-SI (QSI) is the leading solution for integrated signal integrity, timing and crosstalk analysis of high-speed parallel interfaces. SiSoft’s products automate comprehensive pre- and post-route analysis of high speed interfaces, detailing a design’s operating voltage and timing margins. More information on SiSoft can be found at www.sisoft.com.

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